

Date Byte Insertion Circuitry

ABSTRACT OF THE DISCLOSURE

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A data byte insertion circuit includes circuitry to generate derivative intermediate data words from input data words of a current and a preceding cycle, repositioning data bytes of the input data words before and after data byte insertion points of the current and preceding cycles, and circuitry to generate re-aligned variants of insertion data bytes of the current cycle. The data byte insertion circuit further includes circuitry to generate a number of multi-bit data bit selection masks, and circuitry to generate an output data word by conditionally using selected parts of the derivate intermediate data words and the re-aligned variants of the insertion data bytes, in accordance with the multi-bit data bit selection masks.

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